

Hybrid Analog-To-Digital Converter With Fractional/Multi Bit Per Cycle Conversion

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ABSTRACT

Present invention relates to hybrid analog-to-digital (ADC) converter with fractional or multi bit per cycle conversion, comprising of a quantization stage with at-least two comparator circuit to quantize input to at-least three different voltage zones; at least two Digital-to-analog Converters (DACs); a successive approximation stage; a digital-to-digital converter; wherein input is sampled, and is used in DAC; wherein DAC outputs are used by the comparators; wherein VCM is a common mode input voltage used by DACs as comparison reference (CR) voltage; wherein SAR output is also provided to DAC in each conversion loop; wherein a successive approximation register (SAR) is used to generate, and store comparator outputs in different SAR loops of single conversion cycle; wherein a digital-to-digital converter is used to convert the SAR output to an equivalent binary output; wherein DAC uses SAR outputs to generate offset in the sampled input signal in each SAR loop.

KEY APPLICATION AREAS

1. Analog-to-Digital Converter (ADC) design.
2. Low-power embedded electronics.
3. IoT and edge devices.
4. Biomedical and body sensor systems.
5. Mixed-signal integrated circuits (ICs).

POTENTIAL USE

1. Wearable health and physiological monitoring devices.
2. Battery-powered IoT sensors and edge nodes.
3. Low-power data acquisition systems.
4. Portable medical electronics.
5. Resource-constrained embedded systems requiring fast, energy-efficient signal conversion.