

Method of running an unrolled binary search or multiple level search for pipeline adc

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ABSTRACT

Present invention relates to METHOD OF RUNNING AN UNROLLED BINARY SEARCH OR MULTIPLE LEVEL SEARCH FOR PIPELINE ADC [FIG. 1] comprising of: N comparators, (N-1) SCMA logic blocks, and (N-2) buffers; Switched capacitor multiplexing and addition (SCMA) logic blocks; Dynamic comparators; Clocked buffers; Digital-to-analog converter (DAC); a register bank; a digital control circuit to control the internal operation of the SCMA logic block; and characterized in that, an adjustable input-queued binary split algorithm (AI-QBSA) functionalized to convert an analog input signal into an equivalent N bit of digital data wherein, the N-bit output is obtained with the help of "n" stages: wherein $n = N-1$; wherein each nth stage is comprised of an SCMA logic block and a comparator, along with an LSB comparator.

KEY APPLICATION AREAS

1. Analog-to-digital converters (ADCs).
2. High-speed data acquisition systems.
3. Communication systems.
4. Medical imaging and particle detectors.
5. Industrial sensing and instrumentation.
6. Low-power embedded electronics.

POTENTIAL USES

1. High-speed, high-resolution analog-to-digital conversion.
2. Energy-efficient signal processing.
3. Data acquisition for medical and space applications.
4. Mobile, wireless, and sensor devices.

5. Real-time digital conversion in communication systems.
6. Low-power, high-throughput electronic systems.